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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,247	09/24/2003	Mitsuaki Osame	0756-7202	2065

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,247	OSAME ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25 and 27-32* is/are allowed.

6)☒ Claim(s) *1-5,11-16 and 26* is/are rejected.

7)☒ Claim(s) *6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 11-16 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Osame (US 2003/0210219 A1).

The applied reference has a common assignee or inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Osame teaches all claimed features in Fig. 1, a clocked inverter comprising: a first transistor (101) and a second transistor (102) connected in series, and a third transistor (105) and a fourth transistor (103) connected in series, and a fifth transistor (106) and a sixth transistor (104) connected in series wherein: gates of the third transistor and the fourth transistor are connected to each other (at LAT), drains of

the third transistor and the fourth transistor are each connected to a gate of the first transistor (as seen coupling to gate of 101), sources of the first transistor (101) and the fourth transistor (103) are each electrically the connected to a first power source (VDD), sources of the second transistor (102) and the sixth transistor (106) are electrically connected to a second power source (VSS), and gates of the fifth transistor (106) and the sixth transistor (104) are connected to each other (at LATB), drains of the fifth transistor and the sixth transistor are each connected to a gate of the second transistor (solid node on the gate of 102), and an amplitude of a signal (DATA) inputted to a source of the third transistor (105) is smaller ([0048], High potential of data signal is 6V) than a potential difference between the first power source and the second power source (9V minus 0V equals 9V), and an amplitude of a second signal inputted to a source of the fifth transistor (106) is smaller ([0048], low potential of data signal is 3V) than the potential difference between the first power source and the second power source.

In claim 1, Osame teaches all claimed features in Fig. 1, a clocked inverter comprising: a first transistor (102) and a second transistor (101) connected in series, and a third transistor (106) and a fourth transistor (104) connected in series, and a fith transistor (105) and a sixth transistor (103) connected in series, wherein: gates of the third transistor and the fourth transistor are connected to each other (at LATB), drains of the third transistor and the fourth transistor are each connected to a gate of the first transistor (as seen coupling to gate of 102), sources of the first transistor (102) and the fourth transistor (104) are each electrically the connected to a first power source (VSS), sources of the second transistor (101) and the sixth transistor (103) are electrically

connected to a second power source (VDD), and gates of the fifth transistor (105) and the sixth transistor (103) are connected to each other (at LAT), drains of the fifth transistor and the sixth transistor are each connected to a gate of the second transistor (solid node on the gate of 101), and an amplitude of a signal (DATA) inputted to a source of the third transistor (106) is smaller ([0048], High potential of data signal is 6V) than a potential difference between the first power source and the second power source (9V minus 0V equals 9V), and an amplitude of a second signal inputted to a source of the fifth transistor (105) is smaller ([0048], low potential of data signal is 3V) than the potential difference between the first power source and the second power source.

In claim 2, Osame further teaches the clocked inverter according to claim 1, wherein: the first power source is a high potential power source (VDD); the second power source is a low potential power source (VSS); the first transistor (101), the fourth transistor (103) and the fifth transistor (106) are each a P-type transistor (as seen); and the second transistor (102), the third transistor (105) and the sixth transistor (104) are each an N-type transistor (as seen).

In claim 3, Osame further teaches the clocked inverter according to claim 1, wherein: the first power source is a low potential power source (VSS); the second power source is a high potential power source (VDD); the first transistor (102), the fourth transistor (104) and the fifth transistor (105) are each an N-type transistor (as seen); and the second transistor (101), the third transistor (106) and the sixth transistor (103) are each a P-type transistor (as seen).

In claim 4, Osame further teaches the clocked inverter according to claim 1,

wherein the third transistor is replaced with an analog switch [paragraphs 0029 and 0031].

In claim 5, Osame teaches all claimed features in Fig. 4, a clocked inverter comprising: first to third transistors (101, 201, 202) connected in series, and a fourth transistor and a fifth transistor (105, 103) connected in series, wherein: gates of the fourth transistor (105) and the fifth transistor (103) are connected to each other (at LAT); drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor solid node on the gate of 101); sources of the first transistor (101) and the fifth transistor (103) are each electrically connected to a first power (VDD); sources of the third transistor (202) is electrically connected to a second power source (VSS via 102); and an amplitude of a signal inputted (DATA) to a source of the fourth transistor is smaller ([0048], High potential of data signal is 6V) than a potential difference between the first power source and the second power source.

In claim 11, Osame teaches all claimed features in Fig. 4, a NAND comprising: a first transistor (101) and a second transistor (201) connected in series; a third transistor (102) connected to the first transistor and the second transistor in series (via 202); and a fourth transistor (106) and a fifth transistor (104) connected in series, wherein: gates of the fourth transistor and the fifth transistor are connected to each other (LATB); drains of the fourth transistor and the fifth transistor are each connected to a gate of the third transistor (102); sources of the first transistor (101) and the second transistor (201) are each electrically connected to a first potential power source (VDD); sources of the third transistor (102) and the fifth transistor (104) are each electrically connected to a

second potential power source (VSS); and an amplitude of a signal (DATA) inputted to a source of the fourth transistor and each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor is smaller [0048] than a potential difference between the first potential power source and the second potential power source.

In claim 12, Osame further teaches the NAND according to claim 11, wherein: the first power source is a high potential power source (9V); the second power source is a low potential power source (0V); and the first transistor (101), the second transistor (201), and the fourth transistor (106) are each a P-transistor, and the third transistor (102) and the fifth transistor (104) are each an N-type type transistor.

In claim 13, Osame further teaches the NAND according to claim 11, wherein the fourth transistor is replaced with an analog switch ([0029 and [0031]).

In claim 14, Osame teaches all claimed features in Fig. 4, A NOR comprising: a first transistor (102) and a second transistor (202) connected in series; a third transistor (101) connected to the first transistor and the second transistor in series (via 201); and a fourth transistor (105) and a fifth transistor (103) connected in series, wherein: gates of the fourth transistor and the fifth transistor are connected to each other (at LAT); drains of the fourth transistor (105) and the fifth transistor (103) are each connected to a gate of the third transistor (to the gate of 101); sources of the first transistor and the second transistor are each electrically connected to a first potential power source (VSS); sources of the third transistor (101) and the fifth transistor (103) are each electrically connected to a second potential power source (VDD); and an amplitude of a

signal (DATA) inputted to each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor and to a source of the fourth transistor is smaller [0048] than a potential difference between the first potential power source and the second potential power source.

In claim 15, Osame further teaches the NOR according to claim 14, wherein: the first power source (VSS) is a low potential power source (0V) the second power source (VDD) is a high potential power source (9V): and the first transistor (102), the second transistor (202), and the fourth transistor (105) are each an N- transistor, and the third transistor (101) and the fifth transistor (103) are each a P-type type transistor.

In claim 16, Osame further teaches the NOR according to claim 14, wherein: the fourth transistor is replaced with an analog switch ([0029] and [0031]).

In claim 26, Osame further teaches the clocked inverter according to claim 1, wherein the fifth transistor is replaced with an analog switch [paragraphs 0029 and 0031].

3. Claims 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 17-25 and 27-32 appear to comprise allowable subject matter(s) of a plurality of stages, an inverter, and an analog switch.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 5, 11 and 14 have been considered but are moot in view of the new ground(s) of rejection.

As discussed in great detail above, the reference of Osame, US 2003/0210219, anticipates claims 1-5, 11-16 and 26 under 35 U.S.C. 102(e), having a common assignee or inventor.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIBOL TAN
PRIMARY EXAMINER